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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
QI, ZHI QIANG

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,364	LAI, HAN-CHUNG	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005 and 21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-6 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-6 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-5 and 10-14 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,310,668 B1 (Ukita).

Regarding claims 1, 5 and 11, Ukita discloses (col.4, line 29 – col.6, line 21; Fig.11) that a liquid crystal display device with a capacitance-compensated structure comprises:

- gate line (33);
- gate (32) electrically connected to the gate line (33);
- compensation structure (such as 61 or a protruded portion of the gate electrode functions also as compensation structure) extending from at least one of the gate and gate line, i. e., extending from the gate (32) or the gate line (33);
- the protruded portion of the pixel electrode (42) functions as drain electrode having a first side (such as left side) opposite to a second side (such as right side), and the first side (left side) of the drain (42) overlaps the gate (32) and the second side (right side) of the drain (42) overlaps the compensation structure (such as 61);

(concerning claim 5)

- gate line (33) and data line (38) to turn the thin film transistor on or off;
- first parasitic capacitor is formed between the first side (left side) of the drain (42) and the gate (32) and a second parasitic capacitor is formed between the second side (right side) of the drain (42) and gate (32) (because the gate line 33 connected to the gate 32) (any two conductive electrodes create parasitic capacitors), and the second parasitic capacitor comprises the second side (right side) of the drain (42) and a compensation structure extending from at least one of the gate and gate line, i.e., the second side (right side) of the drain (42) and a compensation structure extending from the gate (32) or the gate line (33);

(concerning claim 11)

- first process layer comprising a gate line (33), a gate (32) and a compensation structure (such as 61), and the gate (32) is electrically connected to the gate line (33) and the compensation structure (such as 61) connects to the gate (32) (because the compensation structure such as 61 connected to the gate line 33 and the gate line 33 connected to the gate 32);
- second process layer comprising a data line (38), a source (39) (the drain electrode 39 functions also as source electrode) and a drain (42) (protruded portion of pixel electrode 42 functions as drain electrode); and the source and the drain are formed corresponding to both side of the gate (32) respectively

(see Fig.11); and the source (39) is electrically connected to the data line (38); and the data line (38) is substantially perpendicular to the gate line (33);

- there is an acceptable alignment shift range between the first process layer and the second process layer; because when a gate pattern (as first process) and a source pattern (as second process) are vertically or horizontally misaligned in a mask alignment process, would keep the parasitic capacitance between the gate and the source electrode (functions as drain electrode) at a constant value (see col.4, lines 41-52); such that the sum of the capacitance of the first parasitic capacitor between the first side of the drain and the gate and a second parasitic capacitor between the second side of the drain and the compensation structure maintain a substantially constant value within the acceptable alignment shift range.

Regarding claims 4,10 and 14, Ukita discloses (col.4, line 29 – col.6, line 21; Fig.11) that the capacitance-compensated structure comprises two portions, wherein one portion extends from the gate line (such as 61) and the other portion extends from the gate (such as the protruded portion of the gate 32).

Regarding claims 12, Ukita discloses (col.4, line 29 – col.6, line 21; Fig.11) that the capacitance-compensated structure extends from the gate line (such as 61).

Regarding claims 13, Ukita discloses (col.4, line 29 – col.6, line 21; Fig.11) that the capacitance-compensated structure extends from the gate (such as the protruded portion of the gate 32).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ukita in view of US 5,995,178 (Fujikawa et al).

Regarding claim 6, Ukita teaches the invention set forth above except for that a capacitor dielectric layer of the first parasitic capacitor comprises two portions wherein one portion is a stacked structure comprising a gate insulating layer, a semiconductor layer and a channel protection layer, and the other portion is a stacked structure comprising the gate insulating layer and the semiconductor layer; a capacitor dielectric layer of the second parasitic capacitor is a stacked structure comprising the gate insulating layer and the semiconductor layer.

Fujikawa discloses (Fig.19) that a TFT structure comprises the gate insulating layer and the semiconductor layer and that is common and known in the art. The first and second parasitic capacitors of this application are between the drain electrode and the gate electrode and between the drain electrode and the compensation structure (extended from gate electrode and gate line). As shown in the Fig.19 of Fujikawa, such parasitic capacitor would cover two portions for the dielectric layer that is one portion having the gate insulating layer (422), semiconductor layer (423) and channel protection layer (424), and the other portion having the gate insulating layer (422), semiconductor

layer (423). Therefore, the first parasitic capacitor comprises such two portions, the second parasitic capacitor is not at center portion so that the dielectric layer would comprise the gate insulating layer and the semiconductor layer. Such that the TFT structure having gate insulating layer and semiconductor layer that is common and known in the art and Fujikawa as the evidence.

Concerning the TFT structure having channel protective layer, Fujikawa teaches (Fig.19) that the TFT structure having channel protection layer (424) functions as etching stopper so as to protect the channel portion during the etching process (see col.1, lines 57-65).

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Ukita with the teachings of using the TFT structure having channel protective layer as taught by Fujikawa, since the skilled in the art would be motivated for protecting the channel portion of the TFT during the etching process (see col.1, lines 57-65).

Response to Arguments

5. Applicant's arguments filed on Dec.15, 2005 and Feb.21, 2006 have been fully considered but they are not persuasive.

1) The reference Ukita teaches (col.4, line 29 – col.6, line 21; Fig.11) a liquid crystal display device with a capacitance-compensated structure and using same principle for compensating the alignment shift between the gate pattern (firs process) and source pattern (second process) (col.4, lines 41-52), and the protruded portion of

the pixel electrode (42) functions also as a drain electrode and having two opposite sides as shown in Fig.11.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Qi
March 15,2006

ANDREW SCHECHTER
PRIMARY EXAMINER